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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

| EXAMINER | |
|---|---|
| DOLAN, JENNIFER M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/050,427 | PAPPALARDO ET AL. | |
| | Examiner | Art Unit | |
| | Jennifer M. Dolan | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-17 and 34* is/are allowed.

6)☒ Claim(s) *1-4,7-9,18,23,26-30, and 32* is/are rejected.

7)☒ Claim(s) *5,6,10,11,19-22,24,25,31 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. The Affidavit filed on 12/1/03 under 37 CFR 1.131 is sufficient to overcome the U.S. 6,504,422 to Rader et al. and U.S. 6,369,642 to Zeng references.

### *Claim Objections*

2. Claim 34 objected to because of the following informalities: The punctuation in the claim makes it appear that each pumping line includes a switching network, a control circuit, and a phase assigner, rather than that the charge pump as a whole includes the switching network, the control circuit, and the phase assigner. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent No. 407111095 to Tanzawa et al.

Tanzawa discloses a charge pump capable of having multiple stages, comprising: at least two pumping lines (figures 6 and 11), each line including: an input terminal (see figures 6, 9, 11, and 19; N1, Vin); an output terminal (see figs. 6, 9, 11, 19), N2, Vout) having a different voltage than the input terminal; a pumping capacitor (QD1, C2) having a first terminal coupled between

the input and output terminals (figures 11, 19) and a second terminal structured to accept a phase signal (figure 11); a switched diode coupled between the input terminal and the output terminal to disrupt a connection between the terminals (Qn transistors form switched diodes; figures 11, 19); the charge pump further including a switching network (30) coupled between the pumping lines and structures to couple the pumping lines in either a serial or parallel mode (see figure 6).

5. Claims 18 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,121,821 to Miki.

Regarding claim 18, Miki discloses a charge pump capable of having multiple stages, comprising: at least two pumping lines (3 and 4; figures 9, 12); an input terminal for accepting an input voltage (Vcc, column 10, lines 15-25); an output terminal for delivering an output voltage different from the input voltage (Vout); a pumping capacitor (C11, C21) having a first terminal coupled between the input and output terminals and a second terminal structured to accept a phase signal (#4 or #1; figure 9); a switched diode (formed from NJ0 and MJ0) coupled between the input and output terminals; the charge pump further including a switching network (formed from MN1 and the transistor between Vcc and PK0) between the pump lines and coupling the lines in either a serial or a parallel mode (column 10, lines 50-67; figures 8-12).

Regarding claim 23, Miki further discloses an output switched diode (MJ3, NJ3) coupled to the output terminal (figure 9).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 26, 27, 30, and 32 are rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 6,121,821 to Miki or, in the alternative, under 35 U.S.C. 103(a) as obvious over Miki in view of U.S. Patent No. 5,912,560 to Pasternak.

Regarding claims 1 and 26, Miki discloses a charge pump capable of having multiple stages (figure 9), comprising: at least two pumping lines (3 and 4), each line including an input terminal (Vcc) for accepting an input voltage (column 10, lines 15-25), an output terminal (Vout) for delivering an output voltage different from the input voltage (figures 9, 12), a first pumping capacitor (C21, C26) having a first terminal coupled between the input and output terminals (figures 9, 12) and having a second terminal structured to accept a first phase signal (#4); a second pumping capacitor (C22, C27) having a first terminal coupled between the input and output terminals and having a second terminal structured to accept a second phase signal (#2; figures 9 and 12); a first switch (formed from NJO, MJO) coupled between the input terminal and the output terminal; a second switch (formed from MJ3, NJ3) coupled between the input and output terminal; and a third switch (formed from NJ1 and MJ1) coupled between the first terminals of the first and second capacitors; the charge pump further including a switching network (from MN1 and the transistor between Vcc and node PK0) structured to couple the pumping lines either in a serial or parallel mode (column 10, lines 50-67; figures 8-12). The

transistor arrangements (NJ, MJ) are considered to essentially operate as switches, since MOS transistors are commonly used as non-ideal switches. Miki, however, does not specifically teach the use of switches in the charge pumps.

Pasternak discloses that MOSFETs are often used to function as switches, particularly in charge pumps (see column 2, lines 10-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the transistor arrangement of Miki is considered to operate as switches, as is suggested by Pasternak. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use switches in Miki, because switches are required between adjacent stages in a multi-stage charge pump in order to have pre-charging and boosting steps (i.e., to have the charge pump actually function as a multi-stage pump; see Pasternak, column 1, lines 20-60). Since Pasternak further shows that ideal switches cannot be fabricated, and that MOSFETs are typically used in place of "ideal switches" (Pasternak, column 2, lines 10-35), it is well within the purview of a person skilled in the art to note that the transistor arrangements of Miki are non-ideal switches.

Regarding claim 27, Miki discloses that applying signals to a switching network comprises: applying a signal to a switch coupled between individual charge pumps (figures 8-12; column 11, lines 25-50).

Regarding claim 29, Miki discloses that applying a first signal to a first transistor (MN1) causes the pumps to be coupled in a serial fashion (column 11, lines 25-50), and applying a second signal to a second switch (transistor coupling Vcc to PK0 node) causes the pumps to be coupled in a parallel fashion.

Regarding claim 30, Miki discloses connecting the output signal from one charge pump to the input signal of another (figures 8-12).

Regarding claim 32, Miki discloses that the first and second phase signals (#4 and #2) are in opposite phase from each other (figure 7).

8. Claims 1-4, 7, 26-28, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,767,735 to Javanifard et al. in view of Pasternak.

Regarding claims 1, 3, and 26, Javanifard discloses a charge pump capable of having multiple stages (figure 3), comprising: at least two pumping lines (310, 320, 330, etc), each line including: an input terminal (Vpp terminal; figure 3); an output terminal (terminal connected to node 350); and individual charge pump stages (figure 3), the charge pump further including a switching network (formed from switches 130, 131; see figure 1) structured to couple the pumping lines in either a serial or parallel mode (column 2, lines 54-60). Javanifard further discloses that some switches in the switching network are structured to remain open during a charge pumping operation (table 1; figure 3).

Javanifard fails to specify the structure of each charge pump stage.

Pasternak teaches a basic charge pump stage comprising: first and second pumping capacitors (16a, 16b) with a first terminal coupled between the input and output, and a second terminal coupled to a phase signal (CLK, CLKb); a first switch (10) between the input and output, and a second switch (18b) between the input and output to disrupt a connection between an input and output; and a third switch (18a) between the first terminals of the first and second

capacitors (see figures 1A, 1B, 3A, 3B, 4A, 4B). Pasternak further discloses that some switches must remain open during charge pumping operation (figures 1 and 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the charge pump stage of Javanifard has a structure similar to that disclosed by Pasternak. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use the structure taught by Pasternak as the charge pump stage in Javanifard, because Pasternak shows that such a configuration forms a basic and ideal charge pump circuit, which can appropriately operate in both pre-charging and boosting modes in order to boost the maximum supply voltage (see Pasternak, column 1, line 5 – column 2, line 48).

Regarding claim 2, Javanifard discloses that there are at least four pumping lines (figure 3) and that the switching network comprises at least two switches (130 and 131 for each line).

Regarding claim 4, Javanifard discloses an optimal stages finder coupled to the switching network (column 5, lines 58-67; column 7, lines 10-42).

Regarding claim 7, Javanifard discloses a comparison circuit structured to compare a reference voltage to a power supply voltage and generate an output signal (column 7, lines 52-57).

Regarding claim 27, Javanifard discloses applying signals to a switch coupled between two individual charge pumps (table 1; figures 1 and 3).

Regarding claim 28, Javanifard discloses applying a first signal to a first switch coupled between a first and a second charge pump ("130" switch between lines 310 and 320; see figure 3); and applying a second signal to a second switch between a second and a third charge pump ("130" switch between 320 and 330).

Regarding claim 30, Javanifard discloses connecting the output signal from one charge pump to the input signal of another charge pump (figure 3).

9. Claims 8 and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifard in view of Pasternak, as applied to claim 7 above, and further in view of U.S. Patent No. 6,150,835 to Hazen et al.

Javanifard is silent as to the nature of the comparison circuit.

Hazen discloses a comparison circuit comprising: a resistor ladder (502 and 504) coupled to the power supply voltage (410; figure 5), two reference voltages (532 and 531), and a set of comparators (505 and 507). Hazen further teaches that the inputs of the comparators are coupled to the resistor ladders and reference voltages (figure 5), and the outputs are coupled to a signal latching circuit (figure 5).

Hazen fails to disclose a second resistor ladder.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the comparison circuit of Javanifard as modified by Pasternak, such that it includes the resistor ladder and comparators, as taught by Hazen, and such that it further includes a second resistor ladder. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide the comparison circuit taught by Hazen, because Hazen shows that the circuit accurately checks the range into which the voltage falls, and applies the appropriate signals to the charge pump in light of the detected signal (Hazen, column 4, line 45- column 5, line 55). A person having ordinary skill would additionally have been motivated to provide a second resistor ladder, because the second resistor ladder

would act as a voltage divider, such that the 2V and IV reference signals could be provided using the same supplied reference voltage, rather than requiring two separate voltages to be applied, as is appreciated by one skilled in the art.

***Allowable Subject Matter***

10. Claims 12-17 and 34 are allowed.

11. Claims 5, 6, 10, 11, 19-22, 24, 25, 31, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 5, 6, 31, 33, and 34, the prior art of record only suggests providing opposite phases to adjacent stages in the charge pump, rather than providing the same or configurable phases assigned by a phase assigner. Since there is no suggestion in the prior art to control or optimize the phases in order to provide desired input, it is the examiner's opinion that a person having ordinary skill in the art would simply use opposite phases, as is conventional.

Regarding claims 12-17, the prior art only teaches unit configurations using 3 or fewer switches: one between the first capacitor and the input line, one between the two capacitors, and one between the second capacitor and the output, such that all pumping capacitors are used in the charge pump. By providing additional switches, it is possible to separately couple the first and second capacitor to the input and output lines, such that for any pumping operation, either one of the capacitors may selectively not be used. It is the examiner's opinion that such a modification is critical, since it enhances the flexibility of each charge pump stage in providing varying

voltage outputs, and thus it would not have been obvious to a person skilled in the art to add the extra switches.

Regarding claims 10 and 11, the primary reason for allowability is that there is simply no suggestion in the prior art to provide the signal latching circuit as specified, nor is there any feasible means or rational for modifying the latching circuit of Hazen et al. to meet the claimed limitations.

Regarding claims 19-22, 24, and 25, the primary reason for allowability is that there is generally no motivation in the prior art for coupling a reference voltage directly to an auxiliary capacitor connected to the pumping lines. Although reference voltages are often used in the external circuitry for determining the value of the source voltage/input voltage, it is the examiner's opinion that a person having ordinary skill in the art would have no reason for coupling a reference voltage to the output node/auxiliary capacitor

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd